#6
3-24-93

IN THE UNITED STATES PATENT AND TRADE MARKS OFFICE

Applicant: Richard C. Foss et al

Serial No: 07/680,747

Filed: April 5, 1991

Title: METHOD FOR DRAM SENSING CIRCUIT CONTROL

Art Unit: 2502

Examiner: T. Dinh

Our File: 628.30050X00

The Commissioner of Patents
and Trade Marks,
Washington, D.C., 20231
U.S.A.

March 22, 1993

Dear Sir:

This is in response to the office action dated December 21st, 1992 in the above-identified application.

R E M A R K S

The Patent Office has rejected claims 1-5, 16-17 under 35 U.S.C. 112 for the reason that "imperfectly isolating" is unclear. Applicant respectfully traverses the rejection for the following reason. Claim 1, clause (d) identifies the imperfect isolating means "whereby current can leak therethrough". Claim 16, clause (a) defines the function of imperfectly isolating, and clause (c) defines leaking the charge through the imperfectly isolating means, thereby causing a voltage differential to occur.

It is submitted that in the claims the term "imperfectly isolating" is clearly indicated to mean that

there is a means which does not perform perfect isolation. Since an isolating means is a barrier between nodes, an imperfect isolating means would be understood to any person skilled in the art to mean that current can leak between the nodes.

The disclosure introduces the concept of imperfect isolation on page 3, lines 10-25. For example, lines 22-25 state that the imperfect isolation referred to means that the source-drain of the FET (the imperfect isolation device) is in a high resistance state, but allows some charge leakage through the FET.

The term "imperfect isolation" has been clearly defined in the disclosure, and is used in accordance with that meaning in the claims.

It is therefore submitted that claims 1-6, 16 and 17 meet 35 U.S.C. 112. Withdrawal of the rejection is respectfully requested.

Claims 1-17 were rejected under 35 U.S.C. 102(b) as anticipated by Wang ('142), Miyamoto et al ('850) and Miyamoto ('663), taken separately. Applicant traverses the rejection for the following reason.

The Wang reference describes a structure which is precisely what applicant has invented over. Applicant shows isolators 6a and 6b as prior art in Figure 1. This is exactly what is shown in Wang: elements 14. On page 2, lines 35-40 of the reference, it is stated that the bitlines are divided in half by an isolating transistor. There is no

imperfect isolation. The entire objective of the reference is to divide the bitline in half by use of an MOS transistor which perfectly isolates each bitline half.

Thus while the Patent Office is correct that Wang describes and shows isolators 14, he does not show, nor does he consider the significance of imperfect isolation means whereby current can leak therethrough, as defined in claims 1 and 16 and claims dependent thereon.

The Miyamoto et al references teach the same prior art structure noted in applicant's Figure 1, from which applicant's invention distinguishes.

In the '850 reference, isolators Q14 and Q15 divide the bitlines. In the '663 reference, isolators Q73 and QT4 divide the bitlines. The division of the bitlines is described, for example, in column 10, lines 30-47 of the '850 reference and in column 2, lines 39-45 of the '663 reference. Indeed, in the latter reference the isolators are referred to as gates. Gates and isolators which leak would be considered as deficient elements for the purposes of the references.

However in applicant's invention gates and isolators are not used. Rather, leaky isolators are used, to provide a particular function as described in the disclosure. Claims 1 and 16 and their dependent claims specify that current leaks through the imperfect isolating means between the bitline and sense nodes. Nothing similar is described in the references.

A leaky (imperfect) isolator is not an isolator, since it allows current leakage therethrough, while an isolator inhibits any current from passing.

It is believed clear that none of the references appreciate the problem solved by applicant's invention, nor do they teach a combination of elements which solve the problems solved by applicant's invention. In particular, they do not contain key elements in applicant's claims, i.e. imperfect isolating means, which can be disabled thereby removing the imperfect (leaky) isolation.

It is thus clear that the claims are not anticipated in view of any of the cited references. Withdrawal of the rejection and allowance of the claims is respectfully requested.

Claims 7, 8 and 9 were rejected in view of each of the aforenoted references. Applicant does not understand the reason for the rejection.

Claim 7 and its dependent claims define a pair of low resistance power supply conductors extending in parallel with a row of sense amplifiers, for carrying logic high level and logic low level voltages, sense amplifier enabling signal conductors extending across a chip accessible to the sense amplifiers, means for coupling sense inputs of the sense amplifiers to the power supply conductors, and means coupling the sense amplifier and enabling signal conductors to enabling inputs of the means for coupling sense inputs, for enabling passage of current

resulting from the logic high level and low level voltages to the sense amplifiers. This combination is neither described nor suggested in any of the references. Withdrawal of the rejection of claims 7-9 is respectfully requested.

Formal drawings will be submitted upon or prior to notice of allowance.

It is believed that this application is in form for allowance. Notice of allowance is respectfully requested.

To the extent necessary, applicant's petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (628.30050X00) and please credit any excess fees to such deposit account.

Respectfully submitted,

Carl I. Brundidge
Registration No. 29,621
ANTONELLI, TERRY, STOUT & KRAUS

CIB/DRA/cec
(202) 828-0300